DCP3TAPR Project Status (07/10/2010 - 04:09:48)			
Project File:	DCP3TAPR.ise	**Current State:**	Placed and Routed
Module Name:	dcp3	• **Errors:**	No Errors
Target Device:	xc3s500e-4vq100	• **Warnings:**	152 Warnings (152 new)
Product Version:	ISE 10.1.03 - WebPACK	• **Routing Results:**	All Signals Completely Routed
Design Goal:	Balanced	• **Timing Constraints:**	All Constraints Met
Design Strategy:	Xilinx Default (unlocked)	• **Final Timing Score:**	0 (Timing Report)

DCP3TAPR Partition Summary	[-]
No partition information was found.	

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	5,148	9,312	55%	
Number of 4 input LUTs	5,813	9,312	62%	
Logic Distribution				
Number of occupied Slices	4,376	4,656	93%	
Number of Slices containing only related logic	4,376	4,376	100%	
Number of Slices containing unrelated logic	0	4,376	0%	
Total Number of 4 input LUTs	6,214	9,312	66%	
Number used as logic	4,937			
Number used as a route-thru	401			
Number used as 16x1 RAMs	20			
Number used for Dual Port RAMs	96			
Number used as Shift registers	760			
Number of bonded IOBs				
Number of bonded	57	66	86%	
IOB Flip Flops	12			
Number of RAMB16s	20	20	100%	
Number of BUFGMUXs	3	24	12%	
Number of DCMs	1	4	25%	
Number of MULT18X18SIOs	18	20	90%	

Performance Summary				[-]
Final Timing Score:	0	**Pinout Data:**		Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**		Clock Report
Timing Constraints:	All Constraints Met			

Detailed Reports	[-]

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Sat Jul 10 03:58:49 2010	0	89 Warnings (89 new)	10 Infos (10 new)
Translation Report	Current	Sat Jul 10 04:05:40 2010	0	35 Warnings (35 new)	0
Map Report	Current	Sat Jul 10 04:05:59 2010	0	25 Warnings (25 new)	3 Infos (3 new)
Place and Route Report	Current	Sat Jul 10 04:09:36 2010	0	3 Warnings (3 new)	3 Infos (3 new)
Static Timing Report	Current	Sat Jul 10 04:09:48 2010	0	0	3 Infos (3 new)
Bitgen Report					

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