DCP3TAPR Project Status (07/10/2010 - 03:58:51)			
Project File:	DCP3TAPR.ise	**Current State:**	Synthesized
Module Name:	dcp3	• **Errors:**	No Errors
Target Device:	xc3s500e-4vq100	• **Warnings:**	89 Warnings (89 new)
Product Version:	ISE 10.1.03 - WebPACK	• **Routing Results:**	
Design Goal:	Balanced	• **Timing Constraints:**	
Design Strategy:	Xilinx Default (unlocked)	• **Final Timing Score:**	

DCP3TAPR Partition Summary	[-]
No partition information was found.	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4236	4656	90%
Number of Slice Flip Flops	5200	9312	55%
Number of 4 input LUTs	6363	9312	68%
Number of bonded IOBs	56	66	84%
Number of BRAMs	20	20	100%
Number of MULT18X18SIOs	18	20	90%
Number of GCLKs	3	24	12%
Number of DCMs	1	4	25%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Jul 10 03:58:49 2010	0	89 Warnings (89 new)	10 Infos (10 new)
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

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