Simulation & Synthesis of Five Port Router

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Abstract

In the previous paper "Five Port Router for Network on Chip", we design the router for Network on Chip (NoC) design, which was supporting five parallel connections at the same time simultaneously. Since each input channel and output channel of each five port is having its control and decoding logic, so five requests can be granted at the same time by reducing communication bottleneck and thus increases the performance of router. In this paper, we are coding the router in VHDL (VHSIC Hardware Descriptive language) and doing its simulation in modelsim5.1 and its Synthesis in Xilinx 6.1 version.

1. Introduction

As already discussed in previous paper, router is having five ports east, west, north, south and local port. Each port is having its input and output channel, and each input and output channel is having its control and decoding logic, which supports five parallel connections at the same time simultaneously.

The input channel consists of three parts i.e. FIFO, FSM, and XY logic. The FIFO here is used as input buffer to store the data temporarily. It is of 8 bits size and is of depth 16 bits. The first 8 bits of FIFO is header containing the coordinates of destination port, thus the size of packet varies from 8 to 120 bits. FSM is used to control the read and write operation of FIFO, according to its status. If FIFO is empty, FSM generates the signal to perform the write operation and if FIFO is full, FSM generates signal to perform the read operation. XY logic is the deterministic logic which analyzes the header of packet to find out its destination address. XY logic compares the coordinates values stored in header with the locally stored coordinates values and send the data to its destination port.

Similarly the output channel consists of three parts i.e. FIFO, FSM and arbiter. The FIFO here is used as output buffer to store the data temporarily. It is of 8 bits size and is of depth 16 bits the 8 bits are the header, thus the packet size varies from 8 bits to 120 bits. FSM is used to control the read and write operation of FIFO according to its status. If FIFO is empty, FSM generates signal to perform write operation and if FIFO is full FSM generates signal to perform read operation. Arbiter is used in output channel to overcome the problem of multiple input requests coming at single output port. Arbiter is based on rotating priority scheme in which each port get reduced its priority once it has been served.

Cross point matrix consist of multiplexers and demultiplexers and interconnection of all five input ports and output ports. It allows five simultaneous connections at the same time by configuring the input channel and output channel.

2. About VHDL and Software Used

VHDL is the acronym for VHSIC (Very High Speed Integrated Circuits) hardware descriptive language. It is a hardware language that can be used to model a digital system at many levels of abstractions, ranging from algorithmic level to the gate level. It contains elements that can be used to describe the

behavior or structure of the digital system, with the provision for specifying its timing explicitly. The language provides support for modeling the system hierarchically and also supports top down and bottom up design methodologies. It is case insensitive, strongly typed language and is often verbose to write. The models written in this language can be verified using VHDL simulator. Behavioral models that confirms to a certain synthesis description style are capable of being synthesized to gate level description. A model cannot only describe the functionality of design but can also contain information about the design itself in terms of user defined attributes such as total area and speed.

The language used for the coding of router is VHDL in which behavioral and structural style of modeling is used. For simulation purpose the simulator Model sim 5.1 version is used and synthesis purpose Xilinx 6.1 version is used.

3. Implementation

Below is the implementation of five port router in VHDL…….

a. Input FIFO

FFIO is used as input buffer to store the data temporarily. So for coding FIFO there are input signal of it and some output signal from it. The input signals will be data, clock signal, write and read signal. The output signal will be data output, first four bits of header, fifofull and fifoempty signals. If the write signal is high, data will be stored in memory until FIFO is full. There are two counters designed to keep track of read and write operation of FIFO. The output signals fifofull and fifoempty will be given to the input of FSM and the first four bits of header will be the input of XY Logic.

b. Input FSM

FSM is used for controlling the read and write operation of FIFO. The input signal already coming from FIFO are fifofull and fifoempty which shows the status of FIFO, the others input signal will be clock, grant and request signal. The output signals will be write enable read enable, acknowledgement and request signal. When request signal is coming from other router for write operation FSM will check the status of FIFO if it is empty, write enable signal will be high. When FIFO is full and read operation is to be performed, FSM will send the request signal to other router, if grant is received then read enable signal will be high.

c. XY Logic

XY Logic is used for comparing the coordinates stored in header with the locally store coordinates and thus find out the destination address of packet. The input signals will be first four bit of header which is coming from FIFO and the output signal will be requests going to output port. Here the local coordinates are assigned with their values and with the help of XOR function the local coordinates and coordinates stored in header get compare. If the value in X coordinate of header is greater than X coordinate of local stored value then request signal goes to east port otherwise to west port. If both value are equal then Y coordinate is compared, if Y coordinate of header is greater than local stored value then request signal goes to north port otherwise to south port, when both values are equal then request signal goes to local port.

d. Input Channel

In input channel structural modeling is used and FIFO, FSM and XY Logic is included as it component to form complete input channel the input signals are input data, clock signal, request and grant signal. The output signal will be output data, acknowledgement and requests going to all output channels. The port mapping of each component is done here to connect all

e. Output FIFO

FIFO in output channel is used same as in input channel for buffering of data temporarily. The input signals are data, clock signal, write and read signal. The output signals will be data output, fifofull and fifoempty signals, here four bits of header is not considered as it is need not to be analyzed. If the write signal is high, data will be stored in memory until FIFO is full. There are two counters designed to keep track of read and write operation of FIFO.

f. Output FSM

FSM in output channel is same as in input channel which is used for controlling read and write operation of FIFO. The input signal already coming from FIFO are fifofull and fifoempty which shows the status of FIFO, the others input signal will be clock, grant and request signal. The output signals will be write enable read enable, acknowledgement and request signal. When request signal is coming from other router for write operation FSM will check the status of FIFO if it is empty, write enable signal will be high. When FIFO is full and read operation is to be performed, FSM will send the request signal to other router, if grant is received then read enable signal will be high.

g. Arbiter

Arbiter is used in output channel to overcome the problem of multiple input requests coming at single output port. It is based on rotating priority scheme so that each channel request can be served once the input signals are requests coming from all input ports and the output signal will be grand signal to input signal according to its priority.

h. Output Channel

In output channel structural modeling is used and FIFO, FSM and Arbiter is included as its component to form complete output channel. The input signals are input data, clock signal, acknowledgement and requests coming from different input channels. The output signals are data output request and grand signal to input channels according to its priority. The port mapping of each component is done here to connect all.

i. Cross point matrix

Cross point matrix is used for configuring the input channel and output channels the input signals are five data input from five input channels and five select signals. The output signals are five data output for each of the output channel.

j. Routers:-

In router structural modeling is used in which input channel of all 5 ports, output channel of all 5 ports and cross point matrix is used as component to form complete router. The input signals here are five data input signals, five requests signals, and five acknowledgement signals. The output signals are five data output signals, five acknowledgement signals and five request signals. The port mapping of each component is done to connect all.

4. Simulation

Simulation refers to the verification of a design, its function and performance. It is process of applying stimuli to a model over time and producing corresponding responses from a model.

Figure represents the simulation of input channel, output channel and router using Modelsim 5.1 version.

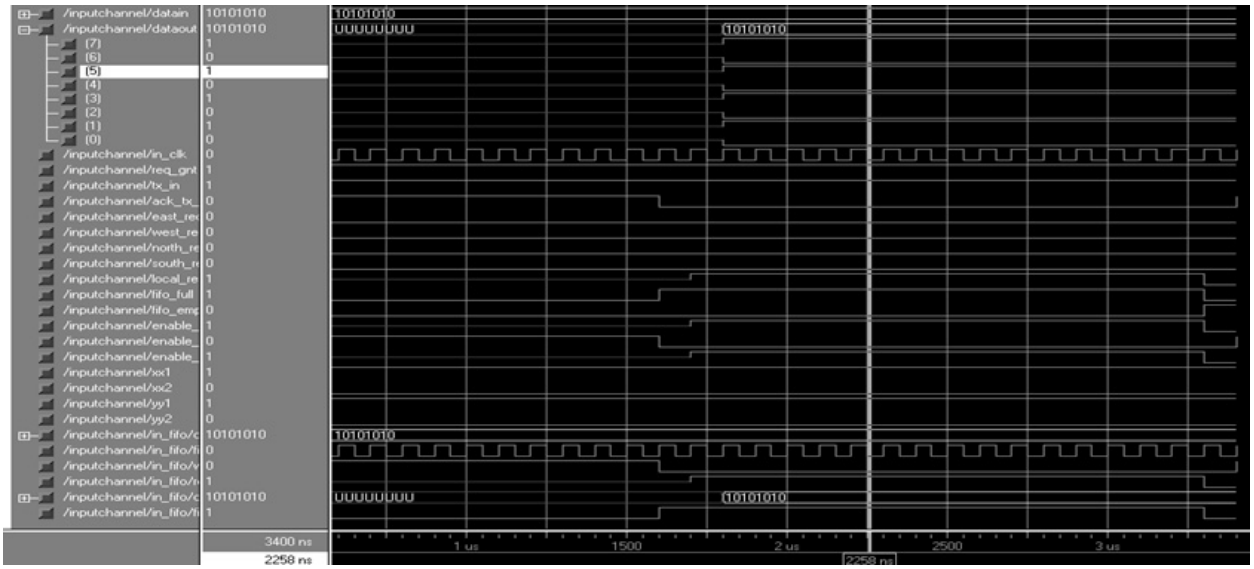

Figure 1 Simulation of Input Channel

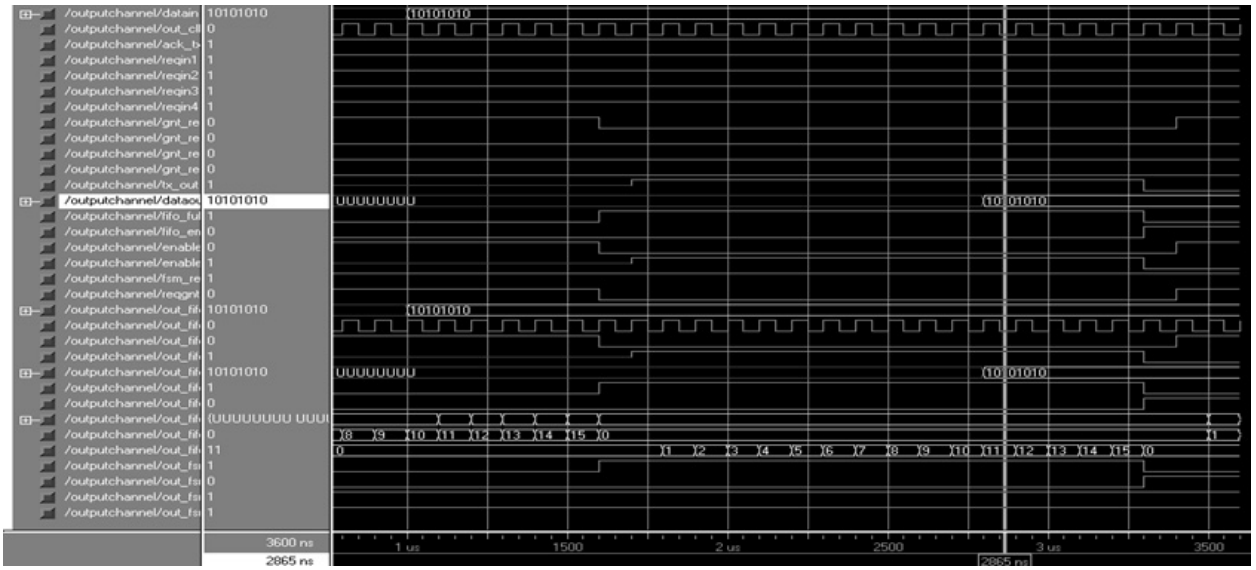

Figure 2 Simulation of Output Channel

5. Synthesis

Synthesis process converts user's hardware description into structural logic description. It provides a means to covert schematics of HDL into real world hardware. Synthesis tools convert the described hardware into a net list that a vendor may use to create a chip or board.

Figure represents the synthesis of input channel, output channel and crosspoint matrix using Xilinx 6.1 version.

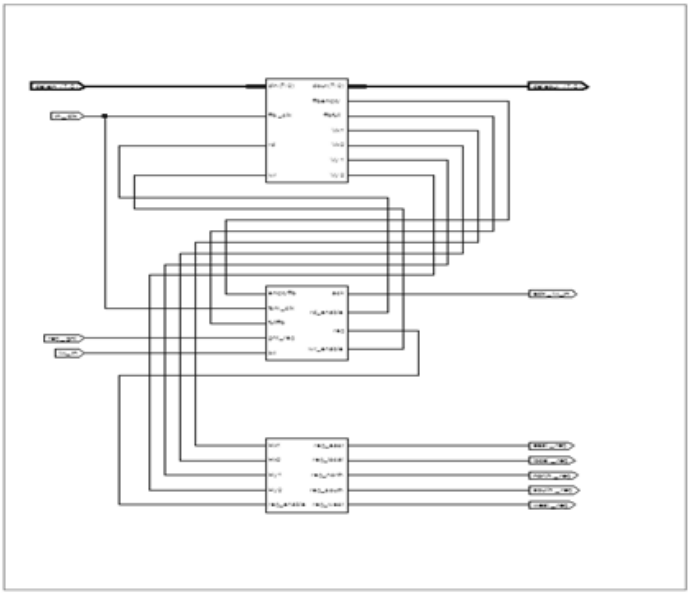

Figure 3 Synthesis of Input Channel

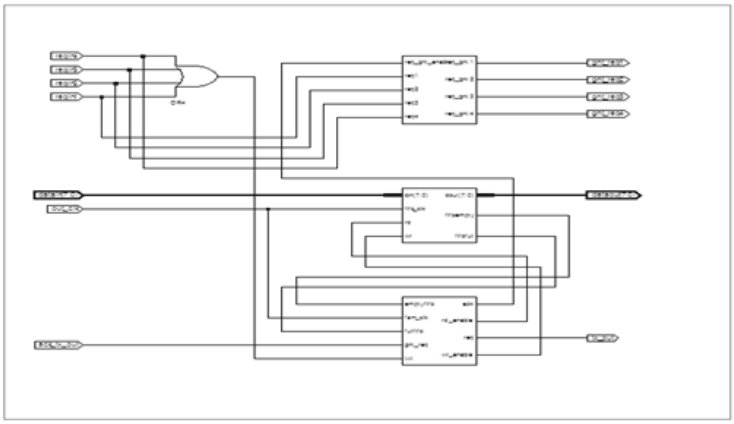

Figure 4 Synthesis of Output Channel

6. Conclusion

Finally after using/implementing above steps we get a synthesis and simulation repot of five port router with the help of Modelsim 5.1 version and Xlinix 6.1 version, that help in understanding proper functioning of Five port router for network on chip.

7. References

1. J. Bhasker, A VHDL Primer, 3rd Edition, Pearson Education, 1998
2. D.M. Chapiro Globally Asynchronous Locally Synchronous Systems. PhD thesis, 1984.
3. W. J. Dally and B. Towles. Route Packets, Not Wires: On-Chip Interconnection Networks. In Design Automation Conference, pages 684–689, 2001.
4. J. Duato and L. Ni S. Yalamanchili. Interconnect Networks: An Engineering Approach. In IEEE CS Press, 1998.

5. Fernando Moraes et. al. A Low Area Overhead Packet-switched Network On Chip:
6. Architecture and Prototyping. In IFIP VLSI-SOC 2003, pages 318–323, 2003.
7. S. Kumar et al. A Network on Chip Architecture and Design Methodology. In Annual Symposium on VLSI'2002, IEEE CS Press, pages 105–112, 2002.
8. Theodore Marescaux et. al. Interconnection Networks Enable Fine-Grain Dynamic Multi-Tasking on FPGAs. In FPL'2002, pages 795–805, September 2002.
9. International Sematech. International Technology Roadmap for Semiconductors - 2002 Update. In http://public.itrs.net, 2002.
10. Xilinx Inc. http://www.xilinx.com, 2004.
11. C.A. Zerferino, M.E. Kreutz, and A.A. Susin. RASoC: A Router Soft-Core for Networks-on-Chip. In DATE'2004-Designer's Forum. IEEE CS Press, 2004.
12. C.A. Zerferino and A.A. Susin. SoCIN: A Parametric and Scalable Network on Chip. In SBCCI'2003, pages 169–174.IEEE CS Press, 2003.