Clock-Block Installation and Operation Manual

Timing and Clock Synthesizer

Revised: 24 March 2007

Introduction

The TAPR Clock-Block is a frequency synthesizer designed for timing and clocking. It accepts a reference input frequency in the range of 2 to 50 MHz and can generate output frequencies from 5MHz to 250 MHz. (Actually, that is the manufacturer's specification, and experiments have shown that a significantly wider frequency range is possible. Operation below 400 kHz and above 400 MHz is possible under the right conditions.)

The Clock-Block requires an input voltage from 7 volts (5 volts when using 3.3 volt logic levels) to 20 volts DC. Typical power consumption is less than 40 ma.

One common application for the Clock-Block is to replace the oscillator in a personal computer to provide a more accurate system clock.

The Clock-Block is designed primarily for timing and clocking applications. It's not intended for use as an RF generator, and its phase noise is not suitable for use in most radio applications.

If you interface your Clock-Block to a specific brand/model of PC motherboard, please send the details to n8ur@tapr.org so that we can add the information to this manual.

Circuit Description

The Clock-Block is built around an ICS525-02 synthesizer chip.

The external reference signal is coupled from J2 to the '525 input pin through C1. This provides DC isolation. The input can be a sine or square wave; its amplitude should be at least 0.5 volts and can be up to the chip operating voltage (either 3.3 or 5 volts). If jumper JP3 is installed, the input will be terminated in 50 ohms. Otherwise, the input is at least 100kohm impedance.

The output of the ICS525 is a square wave with a peak voltage about equal to the regulator voltage. To allow interfacing with different logic families, the Clock-Block contains both 3.3 and 5.0 volt regulators. The desired operating voltage is selected with JP1. Note that operating at 3.3 volts will somewhat reduce the maximum output frequency.

The ICS525 has three dividers which determine the output frequency for a given input frequency:

- A 7-bit divider (switches R0 through R6) between the reference input and the phase comparator.
- A 9-bit divider (switches V0 through V8) between the VCO output and the phase comparator.
- A 3-bit divider (switches S0 through S2) between the VCO and the output pin.

The easiest way to determine the divider settings for a given input and output frequency is to use the calculator provided at ICS' web site: http://www.idt.com/?app=calculators&device=525_01. Be sure you use the results for the -02 version of the chip; the -01 has slightly different programming.

The calculator page will only allow you to enter frequencies within the chip's nominal operating range. If you want to try pushing the chip's limits, or experiment with other divisor combinations, the output frequency is given by:

$$F_{out} = F_{in} * 2 * (V+8) / ((R+2) * S)$$

The V and R dividers are binary coded. The output divider (S0-S2) is not. Its settings are:

Divisor	S0	S1	S2
1	1	1	0
2	0	0	1
3	1	1	1
4	0	1	1
5	1	0	0
6	0	0	0
7	1	0	1
8	0	1	0

The divisor pins have internal pull-up resistors, so ***a logic "0" is represented by a CLOSED switch***. When programming the Clock-Block, it's easiest to start with all switches in the ON position, and turn OFF only those switches that require a logic "1" (most configurations have more "0" than "1" settings).

The following table shows programming information for some common frequencies. All switches are closed (logic 0) other than those listed.

Output Frequency	5 MHz Reference	10 MHz Reference
3.579545545... MHz (use DIV 16 output)	R0, R3, V1, V4, V5, V6, V8	R0, R3, V0, V2, V4, V5, V7
14.318182... MHz	S1, R0, R3, V1, V2, V4, V5, V6	S1, R0, R3,V0, V1, V2, V4, V5
20.000 MHz	R0, V2, V4, V5	S1, V3
33.333333 MHz*	V5	V2, V3
50.000 MHz	S1, V3, V6	S1, V5
100.000 MHz	S0, S1, V3, V6	S0, S1, V5
200.000 MHz	S0, V3, V6	S0, V5
250.000 MHz	S1, S2, V1, V3, V5	S1, S2, V0, V4

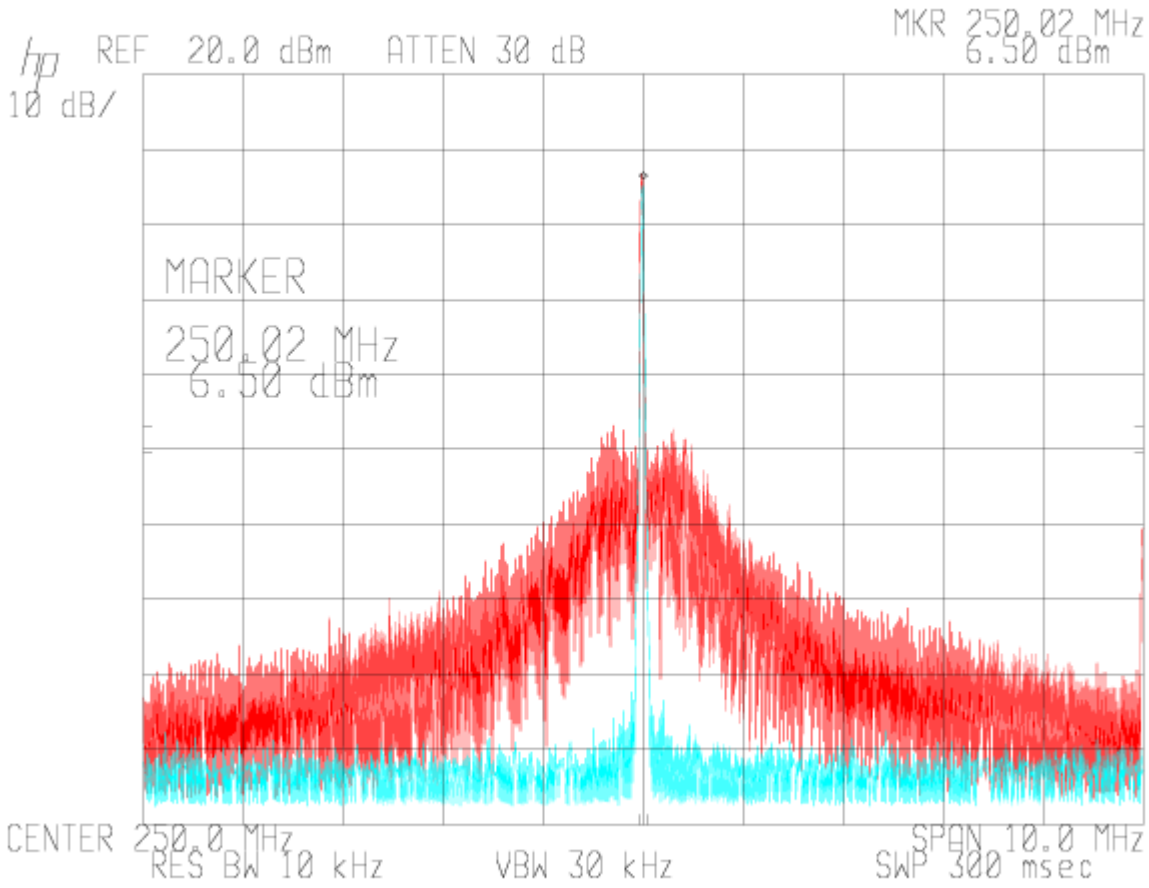
If you'd like to know more about programming and using the ICS525, reference to the data sheet (available at http://www.icst.com/pdf/ics5250102.pdf is highly recommended.

Jumper JP2 normally routes the synthesizer output frequency to connector J3, but by setting that jumper to the "DIV" position, the output is routed to a 74HC4020 binary ripple counter. Six divider ratios are available at jumper block SV1: 16, 64, 256, 1024, 4096, and 16384. By shorting the appropriate pair of holes on the jumper block, the divided frequency will be available at J4. The '4020 chip will work at a maximum input frequency of about 50 MHz. If we assume the manufacturer's specification of a minimum output frequency of 3.75 MHz, the divider output has a range of 228 Hz (3.75 MHz/16384) to 781 kHz (50 Mhz/16). Given that

* To generate 33.333... MHz from a 1 MHz input, set V6 and V7 open, all other switches closed.

the output in practice can be significantly lower than 3.75 MHz, the Clock-Block is capable of a continuous output frequency range from less than 100 Hz to more than 250 MHz. Unfortunately, it's not possible to generate a precise 32.768 kHz output; the best the ICS calculator can do is about 11 parts per million away from that frequency.

Note that the ICS525, and the Clock-Block, are designed for timing, and not RF, applications. The phase noise of the synthesizer is not very good, and it can vary dramatically depending on the divider configuration. To prove that point, here is a spectrum analyzer dump showing the Clock-Block operating at 250 MHz (red), compared with a Marconi 2202A signal generator (cyan):



Installation

Installation of the Clock-Block in a PC to improve the accuracy of the system clock requires surgery on the motherboard.

NOTE: Modifying your PC's components may void its warranty. TAPR cannot be responsible for any damage that may result. Proceed at your own risk!

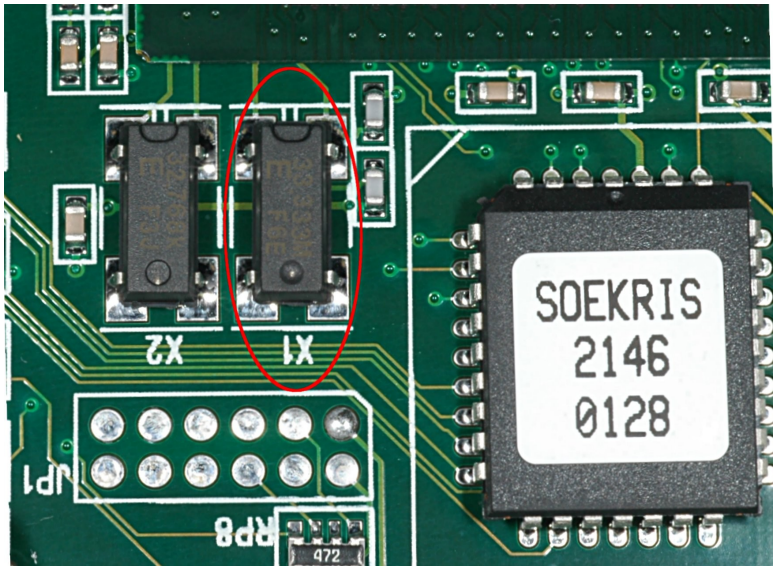
You will need to:

- Find a source of DC power of at least 5 volts;
- Connect the Clock-Block's input to an external reference source; and
- Remove the motherboard's crystal oscillator and replace it with a connection to the Clock-Block output.

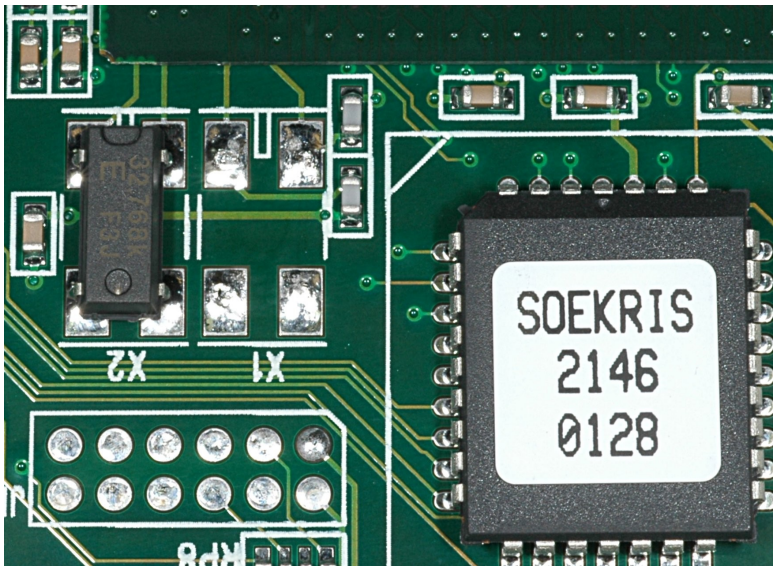
Installation Example – Soekris net4501

The Soekris net4501 single-board computer is commonly used as an NTP time server, and has several features that make it particularly suitable for that task. Here is how I installed a Clock-Block in a net4501.

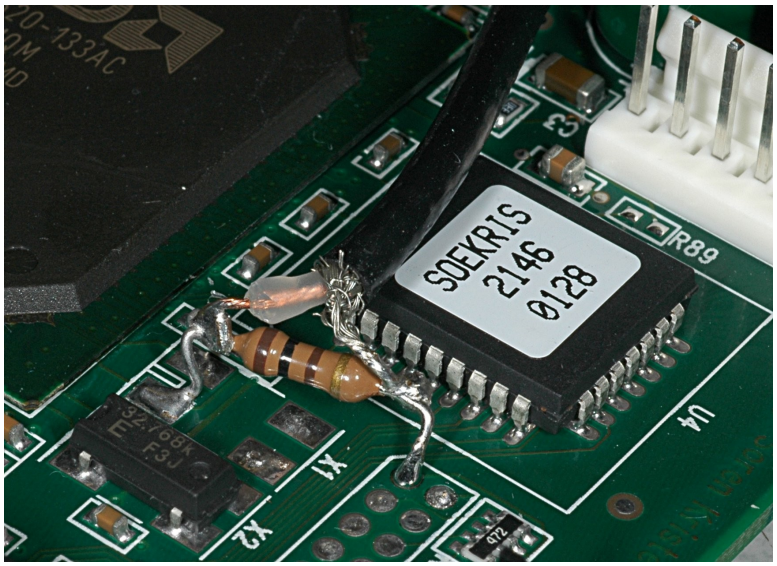
First, find the system clock crystal. It's X1 (33.333 MHz), shown below.



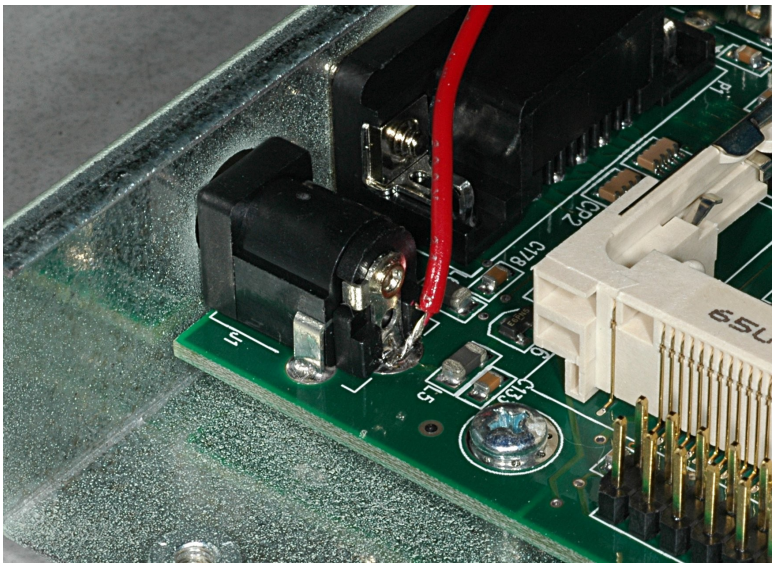
Next, remove X1. A small heat gun is the best way to heat all four pads simultaneously, though with care a soldering iron and solder wick can do the job. If you happen to lift any of the pads, you have three chances out of four that won't be a problem – we'll only be using one pad, the one at the upper left (when looking from the front of the board).



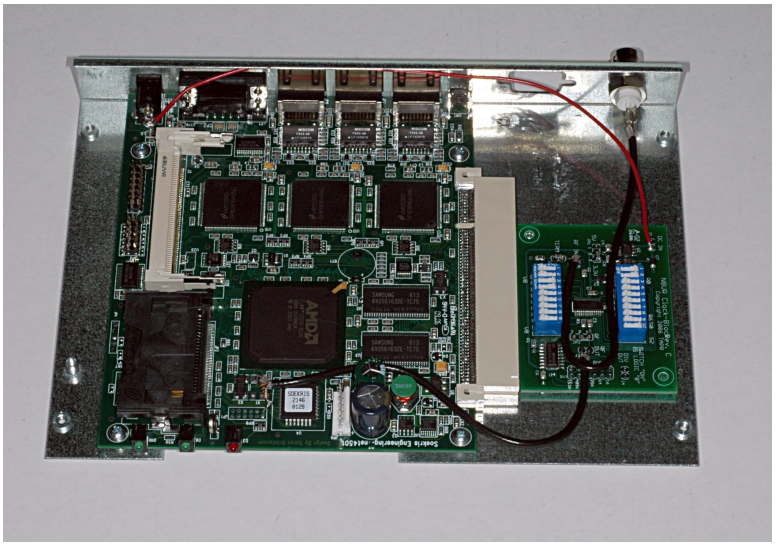
The net4501 CPU uses 2.5 volt logic, so the signal from the Clock-Block, even when using the 3.3 volt regulator, is a little high. A 100 ohm resistor between the clock input and ground will reduce the signal to an appropriate level. The resistor is positioned with one lead on the upper left pad of X1, and the other soldered to the upper right pin of JP3. A piece of RG-174 coax is soldered across the resistor, with the center conductor going to X1, and the braid to the ground at JP3:



Power can be obtained from the Soekris power jack, J1:

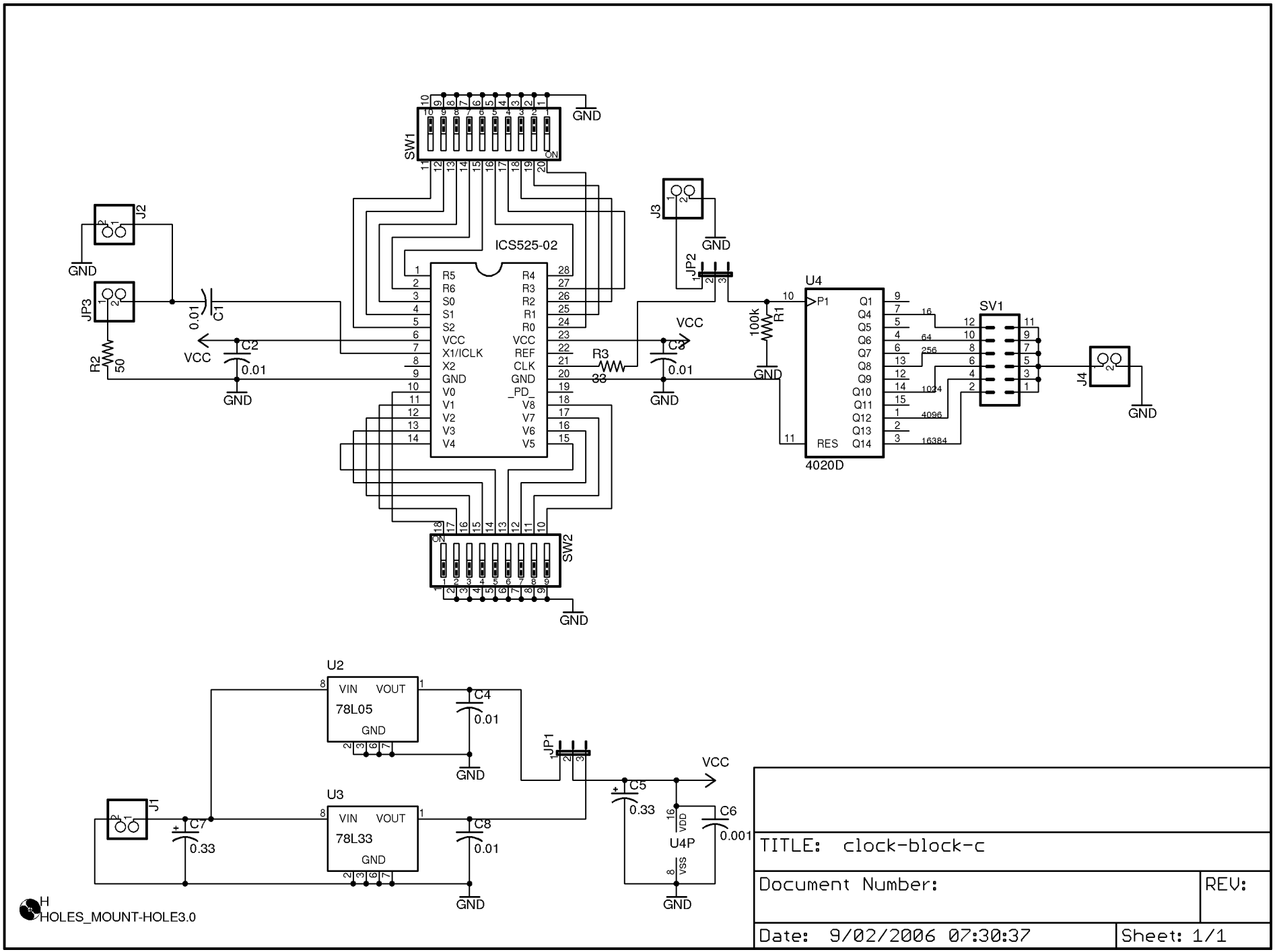


Finally, here's what it looks like when it's all put together:



The Clock-Block needs to generate 33.333333 MHz, so set the jumpers according to the table above.

The reference input comes from a BNC connector mounted to the rear panel of the Soekris case. (Note the the extra DB-9 cutout; that's to support the second serial port which is used for the PPS signal input. If you look carefully, you'll also note that this Clock-Block board looks a little different. It's built without the normal Molex connectors to save height, which is tight in the Soekris case.)



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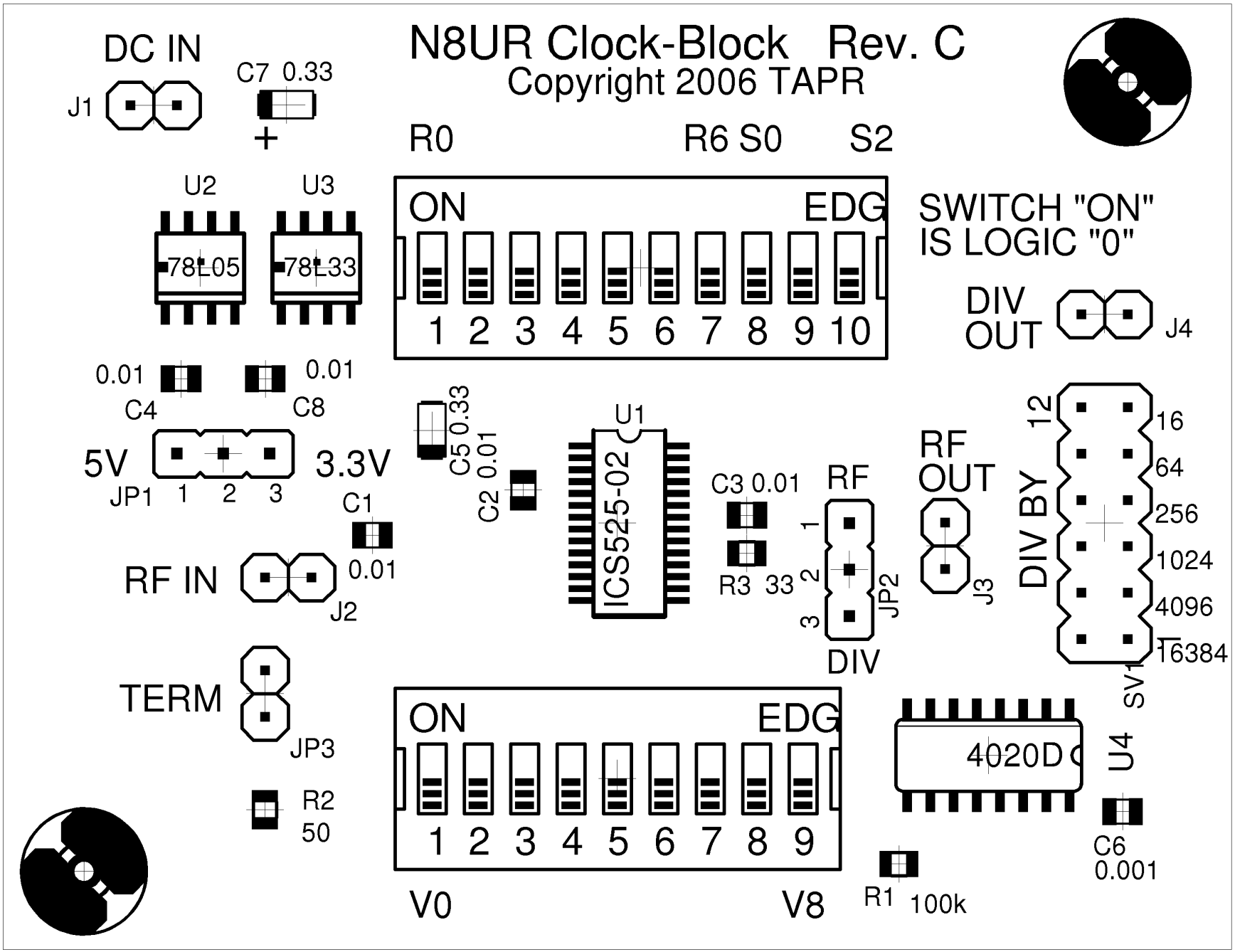
N8UR Clock-Block Rev. C
Copyright 2006 TAPR
DC IN
J1
C7 0.33
+
R0
R6 S0
S2
ON
EDG
1 2 3 4 5 6 7 8 9 10
SWITCH "ON"
IS LOGIC "0"
U2
U3
78L05
78L33
DIV
OUT
J4
0.01
C4
0.01
C8
C5 0.33
C2 0.01
U1
ICS525-02
C3 0.01
R3 33
RF
OUT
J3
RF
1
2
3
JP2
DIV
DIV BY
12
16
64
256
1024
4096
16384
SV1
5V
JP1
1 2 3
3.3V
C1
0.01
RF IN
J2
TERM
JP3
R2
50
ON
EDG
1 2 3 4 5 6 7 8 9
V0
V8
4020D
U4
C6
0.001
R1
100k